Amendments to the Specification:

Please replace the paragraph on page 5, lines 3-16, with the following amended paragraph:

Resistor 25 is a poly resistor that keeps transistor 21 from entering into the saturation region and therefore helps to make the I-V characteristics of ODT resistor 20 more linear. In another embodiment, if the requirement for linearity is not strict, resistor 25 can be a PMOS transistor with its gate connected to ground. In other embodiments, resistor 25 may be another type of resistor such as an N_well, P diffusion or N diffusion resistor. The linearity of ODT resistor 20 is further improved by the current path formed by transistors 22 and 23. ODT resistor 20 can be turned off by applying V_{cc} (a power terminal of the silicon ~~dye~~die) to bias terminal 27. In one embodiment, bias terminal is coupled to the power supply (or ground if NMOS transistors are used) to provide stabilization.

Please replace the paragraph on page 7, lines 1-10, with the following amended paragraph:

Fig. 5 is a graph illustrating the R-V characteristics for ODT resistor 20 at different process corners and temperature, with Vcc=1.2V. Line 40 is a fast process corner at 0C, line 41 a fast corner at 85C, line 42 a typical corner at 85C, and line 43 a slow corner at 110C. It can be seen that, except for a fast corner and 0C (line 40), the ODT resistance is within 45 ohms +/- 2_ohms. The gate bias range is from 0.18V at a ~~fast~~ slow corner and 110C (line 43) to 0.47V at a fast corner and 0C (line [[41]] 40).